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We welcome contributions of original articles, programs, reviews, comments, etc. We are unable to pay for such contributions. We would like to thank all of our subscribers for their assistance–without them this publication would not be possible.

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Ramblings From The Ridge
by D. Sage

We are rapidly approaching the end of another year. I'm afraid that we are also approaching the end of ECN.

It is my intention that our next issue (Issue #24) will be the last regular issue of ECN.

It is possible that we will produce one or two issues beyond that on a less than regular basis, but that won't be decided until later. We therefore will no longer be accepting any renewals or new subscriptions.

If your subscription expires with this issue and you want to receive Issue #24 then simply send us $2.50 and a note indicating that you want Issue #24.

We will resolve all outstanding subscriptions at the time we decide to completely cease publishing.

I am sorry to see this time come, but as each issue passed we began to receive fewer and fewer renewals.

Other factors also added to the necessity for this decision. Changes have also been occurring in my regular job. We are about to undertake a major computerization effort for which I will be responsible and unfortunately it must be accomplished in less time than it will take.

In addition, I have had arthritis for some time and it is becoming more and more difficult for me to work all day and then sit at a keyboard and write.

I have enjoyed the last four years and hope that you will enjoy our remaining issues.

To add to all of the other problems we have experienced, our Zenith computer is sick again. I'm afraid that it may not recover this time.

The only good news is that I now have a bathroom with running water in my office. Unfortunately, I no longer have as much need for an office since we are closing down ECN.

Over the last several years I have built up a file of technical information. Some of this information has already appeared in ECN, so I went through it to see if there was anything I haven't published that you might find useful.

All of this information is now in the public domain, so I will include as much of it as I can over these last two issues.

It is difficult to tell exactly what will end up in this issue, but here are a few additional things that we plan to include: David Clark has sent in some patches for the parallel port more Basic programs and an assembly language program for ADAM CP/M.

We had a few things left over from the last issue (mostly programs) and will include those if possible.

Industry Observations
by D. Sage

The last ten days have seen the stock market go wild. It is difficult to determine what impact this will have on the computer industry. Oddly enough a number of companies recorded higher than anticipated profits just prior to the plunge. It is my opinion that these gyrations will have little impact on the larger successful companies like IBM, Compaq and Apple.

Smaller companies like Commodore that have been experiencing financial problems are more likely to be affected, particularly if they are trying to raise funds through stock offerings. Additionally, if a company sees the value of its stock plummeting, it could find itself a much easier target for a takeover.

This is a problem for companies that have desirable assets or assets that actually exceed the paper value of their stock.

If you could buy a company that has manufacturing facilities worth more than the value of outstanding stock, you could buy the stock and then scrap the rolling stock and come out with a substantial profit. Although this situation does not happen often, it does happen.

If you buy stock for speculation purposes you are taking chances. If you buy stock for the return paid by the company, hold the stock and if the company is profitable in the long run then you have made a good investment. I once knew an investor that had taken out sizable options to buy Coleco stock when it was up around $60 a share. This week the stock was around $6 a share. Two years from now it could go back up to more than its earlier value, but it could also go lower.

Some forecasters are indicating that the current decline of stock values could have a negative impact on the economy. Speculative buying of stocks that resulted in the earlier highs and the recent declines doesn't have to have anything to do with the economy.

If stocks are overvalued and they plummet, it is a crisis for those holding the overvalued stock, but not necessarily for the economy. In actuality, the computers were the ones that panicked and amplified the drop in stocks.

These computers are programmed to automatically buy and sell under certain conditions. When some early declines began to appear in certain stocks, the computers started selling automatically.

They are programmed to minimize total losses while accepting some loss. This meant that they were offering to sell at prices slightly below the going rate in order to move their stocks rapidly. This produced an escalating situation which caused others to begin

selling, producing the unbelievable drops that occurred. It is my opinion that computerized trading (computers issuing buy and sell orders without human intervention) should be prohibited.

On other fronts, Commodore recently appointed Max Toy as president and chief operations officer. Toy was formerly with a division of ITT. I hope he has better luck than his predecessor, Thomas Rattigan. If Irving Gould, CEO and chairman, has any sense at all he will leave the running of Commodore up to someone who knows what they are doing.

Rumors have it that sales of the Amiga are still moving slowly. Commodore is supposed to be planning a major advertising campaign for the Christmas season, but there has been no indication of this here in my area.

Meanwhile, Atari has been developing a transputer based workstation. This system is intended to be ST compatible and operate at a blazing 10 million instructions per second. The operating system will be a UNIX hybrid under development in England. The planned introduction date for the system is late 1988 and the target price is to be below $5000.

The system is scheduled for introduction in Europe first in order to stimulate development of a software base before introduction in the U.S. In addition to supporting the ST operating system the new system will also include a DOS emulator. Atari continues to do the right thing by introducing more and more powerful systems while continuing to provide support for their installed base, providing owners with an upgrade path that allows them to move their software to the new systems. More companies need to pay attention to Atari and follow their example.

Apple continues on their road of profitability and expansion since Steve Jobs departed the company. They are another example of what open architecture and expandability can do for a company. The early Apples were based on that concept and were successful because of that. The Macintosh is now becoming more and more successful since it has returned to an open architecture that allows for third party development and expansion.

Next time I will be bringing you my closing comments on the industry.

Bulletin Board

- **HELP:** Does anyone know if the Smith Corona XD 6500 or XD 6100 can be interfaced to a computer? Also need a replacement carriage control switch for ADAM printer. Contact Noris J. Sparks, 1021 West Second St., Little Rock, AR 72201.
- **QUESTION:** I have a sprite table all set up (10 sprites) and I cannot find a place to put it that it will let me use. Every space that I have tried does something unusual to the operating system. Jason Cwik, 7355 Berkshire Ct., Maple Grove, MN 55369.

Answer: The only places that can be used have to be reserved with either the LOMEM or HIMEM statement in BASIC. You will have to calculate the amount of space needed and then allow for that when you change the memory parameters. It is possible that ten sprites may take up a little too much space.

- **WANTED:** Living outside of the US and am unable to obtain used ADAM products. If anyone can help please send a list and your price to Neil Allen, P.O. Box 132, Pietermarizburg 3200. South Africa.

ADAM Technical Information

This article presents a variety of technical information on the ADAM.

Some of it may be rewritten for clarity and some is presented as it appeared in various source materials, primarily the Technical Reference Manual which is now in the public domain.

Included in this issue is information on the external and internal expansion connectors, power supply, game controllers, memory, port assignments and more.

The following are the device identification numbers used by the ADAM.

These numbers are also used to designate the File Control Block (FCB) device. The values are given in hexadecimal notation.

00H - Master
01H - Keyboard
02H - Printer
03H - Reserved
04H - Disk Drive #1
05H - Disk Drive #2
06H - Reserved
07H - Reserved
08H- Data Drive #1
18H- Data Drive #2
09H - Reserved
OAH - Reserved
OBH - Reserved
OCH - Reserved
ODH - Parallel Interface
OEH - RS-232 Interface
OFH - Gateway

These are the values that many of the system calls need and are identified as FCB_DEVICE. The rest of the technical information is presented in the following pages.

Expansion Port The Expansion Port is conected to the Memory ans I/O Board at P1

TYPE	REFER TO TABLE	PIN	TYPE	REFER TO TABLE
Ground		31	Audio input	
Ground		32	Video input enable +9VDC	
BD3 Tristate, I/O	1, 2	33	NTSC Composite video	
BA14 Tristate, I/O	1, 2		input, 6VDC, 1.5 VAC	
Y2 LS138 decoder output		34	***GAME MODE RESET*** output	
Y1 LS138 decoder output		35	Sound chip 76489 disable,	
HALT	1, 2		0 volts DC	
BWR Tristate output	1, 2	36	Not in use	
NMI input/output	1, 2	37	BA11 Tristate output	1, 2
SPINNER INT DISABLE input	1	38	BA12 Tristate output	1, 2
BUSRQ input	1	39	VDP Sync/Reset input	1
BD1 Tristate, I/O	1, 2	40	***BIORQ*** Tristate output	
Z80 Reset input	1, 2	41	Not used	
BD0 Tristate, I/O	1, 2	42	Not used	1
BM1 Tristate output	1, 2	43	BA15 Tristate output	1, 2
BD7	1, 2	44	BA3 Tristate output	1,2
Tristate, I/O	1, 2	45	B03.58 MHz clock	
BA1 Tristate output	1, 2	46	BD2 Tristate, I/O	1, 2
BD4 Tristate, I/O	1, 2	47	BA0 Tristate output	1, 2
BA2 Tristate	1, 2	48	BD5 Tristate, I/O	1, 2
BA4 Tristate output	1, 2	49	***BRFSH*** Tristate output	
BA13 Tristate output	1, 2	50	***WAIT*** input	1, 2
BA5 Tristate output	1, 2	51	***INT*** input	1, 2
BA6 Tristate output	1, 2	52	***BUSAK*** output	1, 2
BA7 Tristate output	1, 2	53	***BRD*** Tristate output	1, 2
BA8 Tristate output	1, 2	54	***BMREQ*** Tristate output	1
BA9 Tristate output	1, 2	55	***IORQ*** output	1, 2
BA10 Tristate output	1, 2	56	AUDIO 76489 RDY output	
AUX DECODE 1 input	1	57	+12V	
AUX DECODE 2 input	1	58	+5V	
		59	+5V	
Bold Italic denotes active low		60	-5V	

Interconnects - Memory and I/O Board/CPU Board

The Memory and I/O Board is connected to the CPU Board at J1, with two 30-pin ribbon cables and a dual 30-pin card edge connector.

SIGNAL	DESCRIPTION
BDO-DD7	8 bidirectional data lines. BD0 is least significant, BD7 is most significant.
BA0-BA15	16 address lines to Memory and I/O Board. BA0 is least significant, BA15 is most significant.
BWR	Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.
BRD	Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.
BMREQ	Output of Z80 to Memory and I/O Board; indicates present read or write operation is directed to memory or memory-mapped devices.
IORQ ***BIORQ***	Same as ***BMREQ***, but indicates an I/O operation instead of memory or memory-mapped devices.
BRFSH	Output of Z80 to Memory and I/O Board; indicates BA0-BA6 contain a row address for the required dynamic memory refresh. (An eighth row address bit is generated by the MIOC 'RA7'.)
RST	Generated by the MIOC as a result of either a game ***CVRST*** or computer ***PBRST*** reset. It connects to and resets the Colecovision or CPU Board.

Interconnects - Memory and I/O Board/CPU Board (Continued...)

The Memory and I/O Board is connected to the CPU Board at J1, with two 30-pin ribbon cables and a dual 30-pin card edge connector.

SIGNAL	DESCRIPTION
BΦ	System clock generated on Colecovision or CPU Boards. Line connects to Memory and I/O Board.
WAIT	Used to insert extra clock cycles into Z80 timing during opcode fetch cycles and when accessing slow memory or I/O. Excessive use of WAIT causes inadequate dynamic RAM refresh.
ADDRBUFEN	An active low signal enables to address and control signal buffers between the Colecovision or CPU Board, and the Memory and I/O Board. The control signals are ***BRD, BWR, BRFSH, BMREQ, BM1***, and ***BIORQ***. A high level disables these signals from the Z80, and allows them to go tristate (high-impedence). This occurs during a DMA cycle where another device needs to access memory or devices on the emory and I/O Board. See ***BUSRD*** and ***BUSAK***.
245EN	Same as ***ADDRBUFEN*** except ***245EN*** controls the buffer for BD0 through BD7 data lines to CPU or Colecovision buffer board.
BUSRQ ***BUSAK***	***BUSRQ*** (unbuffered) is generated by the MIOC as the result of a DMA request. The ***BUSRQ*** signal requests that the Z80 relinquish the address and data busses and certain control signals at the end of its current cycle. After receiving the ***BUSRQ*** the Z80 responds with a ***BUSAQ*** (buffered) signal to indicate it has relinquished the bus. The Z80 remains in an inactive state until the controlling device removes the ***BUSRQ*** signal. The ***BUSRQ*** line connects to the Colecovision or CPU Board. Generally, only the master 6801 may assert a ***BUSRQ***.
BM1	Output of the Z80 from CPU of Colecovision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).
CVRST	This signal generates an ***RST*** to the Z80 processor. Also reset are the MIOC and master 6801. ***CVRST*** initializes the MIOC memory map such that addresses from 0-1FFFH enable the OS-7 ROM; 2000H through 7FFFH enable the OS-7 ROM; 2000H through 7FFFH enable RAM1; and 8000H through FFFFH enables the game cartridge.
AUXDECODE1	Generated by Memory and I/O Board. Selects or deselects the OS-7 ROM.
INT	Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.
SPINDIS	Allows disabling of spinner interrupts by the hand controllers. Active low.
Audio Out Audio In AUX VID VID GATE CLK, ***RSTDIS*** SEL4, SEL2 ***HALT, NMI*** ***AUXDECODE2*** ***VIDRST***	These signals are not used on the Memory and I/O Board but are made available at the expansion connector.

Card Edge Expansion Connectors

Three card edge connectors are provided for future development.

Connector #1

This connector is soldered to the Memory and I/O Board, and is labeled J7.

Connector #2

This connector is designed for expansion ROM and I/O devices and is soldered to the Memeory and I/O Board. It is labeled J6.

Connector #3

This connector allows for expansion RAM and/or ROM up to 64K bytes, and is labeled J5.

Interconnects for Connector #1 at J7

BD0-BD7 - 8 bidirectional data lines. BD0 is least significant, BD7 is most significant.

BA0-BA7 - Address lines to Memory and I/O Board.

BA0 is least significant, BA7 is most significant.

BWR - Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.

BRD - Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.

IORQ - Same as BMREQ, but indicates an I/O operation instead of memory or memory-mapped devices.
BIORQ

BM1 - Output of Z80 from CPU or Colecovision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).

INT - Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.

Interconnects for Connector #2 at J6

BD0-BD7 - 8 bidirectional data lines. BD0 is least significant, BD7 is most significant.

BA0-BA15 - 16 address lines to Memory and I/O Board. BA0 is least significant, BA15 is most significant.

BWR - Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.

BRD - Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.

BMREQ - Output of Z80 to Memory and I/O Board; indicates present read or write operation is directed to memory or memory-mapped devices.

IORQ - Same as BMREQ, but indicates an I/O operation instead of memory or memory-mapped devices. IORQ is unbuffered; BIORQ is buffered.
BIORQ

BM1 - Output of Z80 from CPU or Colecovision Board; indicates the present memory cycle is an opcode fetch (start of next instruction).

INT - Active low, this signal is an input to the Z80 and results in a maskable interrupt which directs the Z80 to respond to some external event.

Audio In

Interconnects for Connector #3 at J5

BD0-BD7 - 8 bidirectional data lines. BD0 is least significant, BD7 is most significant.

BA0-BA15 - Address lines to Memory and I/O Board. BA0 is least significant, BA15 is most significant. RA7 is substituted for BA7.

BWR - Output of Z80 to Memory and I/O Board; write strobe used to output data during an I/O or memory operation. Indicates a write operation.

BRD - Output of Z80 to Memory and I/O Board; read strobe used to clock data into the Z80 during an I/O or memory operation.

Other Memory and I/O Board Connections

J2 and J8 - AdamNet Connections - The following signals are found on the AdamNet connectors for keyboard and expansion devices.

Data - 62.5K bps serial 'bidirectional' line for data transmission reception by network devices.

Reset - hardware network reset.

+5V

Signal Ground

J9 - Power Supply/Printer Connector - In addition to containing the signals found on J2 and J8, the necessary power supply voltages of +12V Logic, +12V Inductive, and -5V connects here.

J10 and J12 - Data Drive Connectors - For a detailed description of the signals found on the data drive connectors, refer to Subsection 2.3.5.

J1 - Cartridge Connector

PIN	TYPE
1	D2
2	CS3*
3	D1
4	D3
5	D0
6	D4
7	A0
8	D5
9	A1
10	D6
11	A2
12	D7
13	RF Ground
14	All
15	A3
16	A10
17	A4
18	CS1*
19	A13
20	A14
21	A5
22	CS2*
23	A6
24	A12
25	A7
26	A9
27	CS4*
28	A8
29	Digital Ground
30	+5v Typical available current 0.2A

* LS138 Decoder output

Z80 Microprocessor

The Z80 CPU, which consists of a Z80A microprocessor and a clock circuit for synchronization, has control of the Adam computer system.

The Z80 configures the memory map and can switch banks of memory. Refer to Chapter 3, Section 2 for details on the memory configuration.

ROM Circuitry

The CPU Board includes an 8K operating system ROM (OS_7) and a connector for up to 32K of cartridge ROM.

Video Display Processor (VDP)

The Video Display Processor, a Texas Instruments (TI) 9928, generates all video, control and synchronization signals and controls the storage, retrieval and refresh of display data in dynamic memory, VRAM. The 9928 uses a table-driven architecture that allows the programmer to control every pixel in the visual display area, and to define and control 32 "sprites." Sprites may be placed anywhere on the display and moved at will.

The VDP has three major interfaces: CPU, RF modulator, and VRAM. The VDP is addressable in data mode (used when VRAM is being written or read) and register mode (used when control information is being written to and read from one of the VDP's internal registers). The addresses of the ports in the CPU I/O address space are as follows:

Data Port - 0BEH
Register Port 0BFH

The video RAM circuit consists of 8 (16384 x 1) RAM integrated circuits. The contents of VRAM define the TV
image. A0, ***CSW*** and ***CSR*** are CPU-controlled input signals to the VDP that control when the data is written to or read from VRAM. The VDP output signals ***R/W, CAS*** and ***RAS*** control the RAM operation.

Data can be transmitted to or from the CPU over the data bus, depending on the state of the Chip Select Write ***(CSW)*** and Chip Select Read ***(CSR)*** control lines. When ***CSW*** is low, data is transmitted from the CPU to the Video Display Processor. When ***CSR*** is low, data is transmitted from the Video Display Processor to the CPU. ***CSR*** and ***CSW*** should not be simultaneously low.

Another control line, address line A0, determines where the VDP retrieves or sends data. If A0 is in a high state, the data is stored into, or retrieved from an internal register. The register used is determined by the data. If A0 is in a low state, the data is stored into or retrieved from the VRAM.

Refer to the Texas Instruments TMS9918A/TMS9928A/TMS9929A Video Display Processors Data Manual for further information.

Sound Generator

The system uses a TI 76489 (6496) sound generator controller to produce sounds. The chip

contains three programmable tone generators, a programmable white-noise generator, and programmable attenuation for each of the channels. The chip is addressed through a single write-only port at location OFFH. Wait-request hardware has been included in the system because the sound chip is a slow peripheral requiring data lines to be stable for a relatively long time while it is receiving data.

RF Circuitry

The RF modulator uses the 1889 chip to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of two VHF channels, 3 or 4, selectable by a slide switch with determined LC tank circuits. The Chroma subcarrier is derived from the 3.58 MHz system clock to ensure accuracy and stability.

The sound oscillator's frequency modulator is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a varactor diode. Due to the incompatible signal level between the VDP 9928 and the 1889, a DC restoration circuit ensures the DC level of the video signal.

The R-Y, B-Y, and Y signals from the VDP, along with the 3.58 MHz clock and the audio signal from the SN76489 (6496), are provided to the RF modulator to produce the composite video output.

Game Controller Circuitry

The two game controllers are connected to the CPU Board via two "D" type connectors. Each controller is accessed by the system through its own port. See CONT-SCAN In the OS_7 Source Code Listing for details. For each controller, 18 switches are read on a single 8-bit port. Therefore, once a port has been read, some decoding is required to determine which switches have been depressed.

Two spinner switches that are not wired in the controller are used in some games. To ensure that the spinner switch closures are processed as soon as they happen, they are connected to the CPU maskable interrupt, and the cartridge software determines which switch causes the interrupt.

Controller Connector Pin Out

PIN	TYPE
1	Indirect D0 input
2	Indirect D2 input
3	Indirect D3 input
4	Indirect D1 input
5	Strobe signal output, Common 1
6	Indirect D6 input
7	Indirect D5 input
8	Strobe signal output, Common 0
9	Indirect ***INT*** input

Strobe signal: typical 350 micro sec pulse width, -0.7V Low, +2.8V high typ.

Clock Generation

The system clock is a 3.58 MHz square wave generated by dividing the 7.1 MHz clock by two. The video chip clock (10.7 MHz) drives the Video Display Processor. The video chip clock is obtained from the third multiple, high Q tuned tank circuit on the 3.58 MHz system clock. The 7.1 MHz clock is generated by a crystal controlled oscillator. The output of the oscillator circuit is buffered and divided by two to provide a 50% duty cycle wave form.

Interconnects

The CPU Game Board and the Memory and I/O Board connect via two 30-pin ribbon cables and a dual 30-pin card edge connector, making a pin-for-pin connection between J1 on the Memory and I/O Board and J2 on the CPU Board. Refer to Subsection 2.1.9.

POWER SUPPLY

Power Supply Voltage

The power supply for the ADAM computer is located in the printer. The power supply converts the incoming line voltage (AC) to one 18V unregulated voltage that powers the ribbon solenoid and four low level, regulated DC voltages as follows:

+5v	Main source of power to the CPU
-5V	Supplies power to the CPU
+12VI	Supplies power to drive the inductive loads such as carriage motor, daisy wheel motor, print solenoid, platen motor and digital data drive.
+ 12VL	Supplies power to the system logic.

Excessive Current Output Protection

The power supply uses a variety of methods to protect against excessive current output.

The + 5V and the + 12VI are fused and use electronic fold-back current limiting.

The +12VL is not fused but uses electronic foldback limiting.

The -5v uses conventional current limiting and thermal protection which halts the current when the regulator gets too hot.

The 18V unregulated uses the same fuse as the +12VI.

A thermal fuse in the power transformer protects

against overcurrent at the transformer.

The AC line input may vary from 108VAC to 132VAC. The power supply ensures a constant and quiet source of DC power.

Printer/Memory Console Interface Cable

The printer/console Interface cable consists of 7 insulated wires and one uninsulated drain wire.

PIN	COLOR	VOLTAGE DESCRIPTION
1	Brown	12VL VDC +.508V -.6V
2	Red	+12I VDC +.497V -.6V
3	Orange	+5.075 VDC +.079V -.255V
4	Yellow	-5.15VDC +.25V
5	Green	Ground
6	Blue	AdamNet
7	Violet	Reset
8	---	Drain
9	---	No Wire

Power Supply Output to CPU
(via Printer/Memory Console Interface Cable)

VOLTAGE	FULL LOAD CURRENT
+5V	2.75A
-5V	0.2A
+12VI	0.6A
+12VL	0.3A

Power Supply Output to Printer

VOLTAGE	FULL LOAD CURRENT
+5VL	0.25A
+12VI	1.95A
+18V (unreg.)	1.0A

SPECIAL ADAM PRODUCT SALE

Over the last several years I have accumulated a a great deal of hardware and software. Some of these products were purchased fro review and received only limited use. Others are new and others have been used regularly, but were in working condition the last time they were used. Many of the items include their original packaging and all come with their original instructions and necessary software, if any was originally included with the product. The status (usage) of each product is included in the product description. Orders will be filled on a first come, first served basis. To simplify filling orders and or returning payment if necessary, please include a self-addressed stamped envelope. Payment should be check or money order made payable to Sage Enterprises and addressed to Sage Enterprises, ATTN: Special Sale, Rt. 2, Box 211, Russellville, MO 65074. Because of the upcoming holidays please allow 6 to 8 weeks for delivery. If the item being purchased is for Christmas, please identify it as such so that we can be sure to get it to you as quickly as possible. Shipments will not be made until personal checks have cleared, but we will make every attempt to expedite shipping although we have other commitments during these holidays that may cause some delays. Shipping costs are included in all prices.

PRODUCT DESCRIPTION	PRICE
The First Book of ADAM by A. Dent	$7.00
Make-A-Face, Cart, Spinnaker	$5.00
Logic Levels, Cart, Fisher-Price (new)	$5.00
Learning With Leeper, Cart, Sierra (LU)	$5.00
JukeBox, Cart, Spinnaker (LU)	$6.50
Fraction Fever, Cart, Fisher-Price (LU)	$5.00
Dance Fantasy, Cart, Fisher-Price (New)	$5.00
Cabbage Patch Kids - Adventure in Park Cart, Coleco (new)	$5.00
Family Feud, DDP, Coleco (LU)	$10.00
A.E. and Choplifter, DDP, Brodebund (LU)	$10.00
Smartfiler, DDP, Coleco (LU) Updated Ver.	$10.00
Personal Accountant, DDP, Softsync	$7.50
FlashCard Maker, DDP, Coleco (new)	$10.00
ExperType, DDP, Coleco (LU)	$10.00
ADAMLink Modem w/AdamLink 2 software	$50.00
ADAM Daisy Wheel - Pica 10 (new)	$3.00
ADAM Daisy Wheel - Courier (new)	$3.00
ADAM Daisy Wheel - Emphasis (new)	$3.00
ADAM Serial/Parallel Printer Interface with software & serial cable, Eve Electronics (LU)	$60.00
ADAM 64K Memory Expander, Coleco (new)	$40.00
ADAM Keyboard in case, Coleco (new)	$12.00
ADAM Keyboard without case, Coleco (new)	$7.50
Olivetti Jet Ink Printer with extra ink cartridges, Centronics (parallel), (LU)	$80.00
Atari VCS Barely Used - old style, Atari	$25.00
Victory Data Packs (Box of 10)	$15.00
ADAM Data Drive (New)	$15.00
ADAM Data Drives - Groups of 4 (Used)	$17.50
Uncle Ernie's Toolkit, Uncle Ernie (LU)	$15.00
Video Tunes, DDP, Futurevision (LU)	$10.00
Backup+2.0, Disk, MMSG Software (LU)	$10.00

LU - Limited Use